INSTALLATION AND OPERATION

**USER MANUAL**

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# UT986

## GNSS All-constellation Multi-frequency High Precision Timing Module

# Revision History

| Version | Revision History | Date |
|---|---|---|
| R1.0 | First release | May., 2022 |
| R2.0 | Update Table 1-2;<br>Update V_BCKP pin description<br>Add section 3.2 and section 4.1<br>Optimize section 4.2 and section 4.4 | Apr., 2023 |

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# Foreword

This manual provides information about the product characteristics, installation and use, performance indicators and hardware design of the UT986 module.

## Target Readers

This manual applies to technicians who have certain knowledge in GNSS modules.

# Contents

# 1 Product Introduction

UT986 is a new generation of GNSS high precision timing module supporting all constellations and multiple frequencies. It is based on the RF-baseband integrated GNSS SoC — NebulasIV™, and is mainly used in power grids and telecom base station timing.

UT986 has 1408 super channels, supporting BDS (including BDS-3 signals), GPS, GLONASS and Galileo multi-system joint timing and single system standalone timing, which users can flexibly configure. It also supports QZSS and DGPS function.

UT986 module integrates filters and linear amplifiers, and has optimized radio frequency structure and interference suppression capability. With the built-in JamShield adaptive anti-jamming technology and U-AutoAlign multi-path suppression technology, it can detect interference as well as spoofing, ensuring a good performance even in complex electromagnetic environments.

UT986 module can provide nanosecond-level PPS accuracy, support fixed-location timing, optimized-location timing, and positioning timing, and remain good timing accuracy even in complex signal environments.

UT986 features a compact size of 17.0 mm × 22.4 mm × 2.4 mm. It adopts SMT pads, supports standard pick-and-place and fully automated integration of reflow soldering, and is compatible with previous generation of timing products as well as mainstream products on the market.

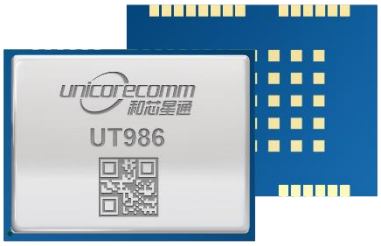


Figure 1-1 UT986 Module

## 1.1 Features

Table 1-1 Product Features

| Model | Grade | | Dimensions (mm) | GNSS | | | | Power (V) | Interface | | | Function | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Industrial Grade | Automotive Grade | | GPS/QZSS | BDS | GLONASS | Galileo | 3.0 to 3.6 | UART1 | UART2 | 1PPS | Built-in Flash | Data Update Rate | DGPS |
| UT986 | • | | 17.0 × 22.4 × 2.4 | • | • | • | • | • | • | • | • | • | 1Hz | • |

## 1.2 Performance

Table 1-2 Key Performance/Specifications

| | |
|---|---|
| **Power** | |
| Voltage | 3.0 V to 3.6 V DC |
| Power Consumption | 700 mW |
| **RF Input** | |
| VSWR | ≤ 3.0 |
| Input Impedance | 50 Ω |
| Antenna Gain | 5 dB to 35 dB |
| **Physical Characteristics** | |
| Package | 28 pin LCC with additional middle ground pads |
| Dimensions | 17.0 mm × 22.4 mm × 2.4 mm |
| Weight | 1.9 g |
| **Environmental Specifications** | |
| Operating Temperature | -40 °C to +85 °C |
| Storage Temperature | -40 °C to +95 °C |
| RoHS2.0 | Compliant |
| **Input/output Data Interface** | |
| UART x 2 | LVTTL, Baud Rate: 9600 bps to 921600 bps |
| **GNSS Performance** | |
| Frequencies | BDS: B1I, B1C, B2a<br>GPS: L1C/A, L2C, L5<br>GLONASS: G1<br>Galileo: E1, E5a, E5b |

| | | | | | |
|---|---|---|---|---|---|
| TTFF[1] | Cold Start: 30 s<br>Reacquisition: 3 s | | | | |
| Positioning Accuracy (CEP)[2] | 1.5 m (Dual-system horizontal, open sky)<br>2.5 m (Dual-system vertical, open sky) | | | | |
| Velocity Accuracy (RMS) | 0.03 m/s (Dual-system horizontal, open sky) | | | | |
| Sensitivity[3] | | GPS | BDS | GLONASS | Galileo |
| | Cold Start | -147 dBm | -145 dBm | -145 dBm | -145 dBm |
| | Tracking | -161 dBm | -160 dBm | -155 dBm | -155 dBm |
| 1PPS Accuracy[4] | 5 ns (1σ) | | | | |
| Data Update Rate | 1 Hz | | | | |
| Data Format[5] | NMEA 0183: Input/Output, ASCII, NMEA4.10, NMEA4.11 (by default) | | | | |
| | Unicore Protocol: Input/Output, ASCII, Unicore Protocol | | | | |
| | RTCM: Input, RTCM3.2 | | | | |

[1] All satellites C/N0 at 41dB

[2] Depends on atmospheric (ionosphere) conditions, GNSS antenna, multipath conditions, satellite visibility and geometry

[3] Tested with a good external LNA at room temperature

[4] Open sky; fixed coordinate system; depends on temperature, atmospheric (ionosphere) conditions, GNSS antenna, multipath conditions, satellite visibility and geometry

[5] Refer to *GNSS Timing Products Protocol Specification*

## 1.3 Block Diagram

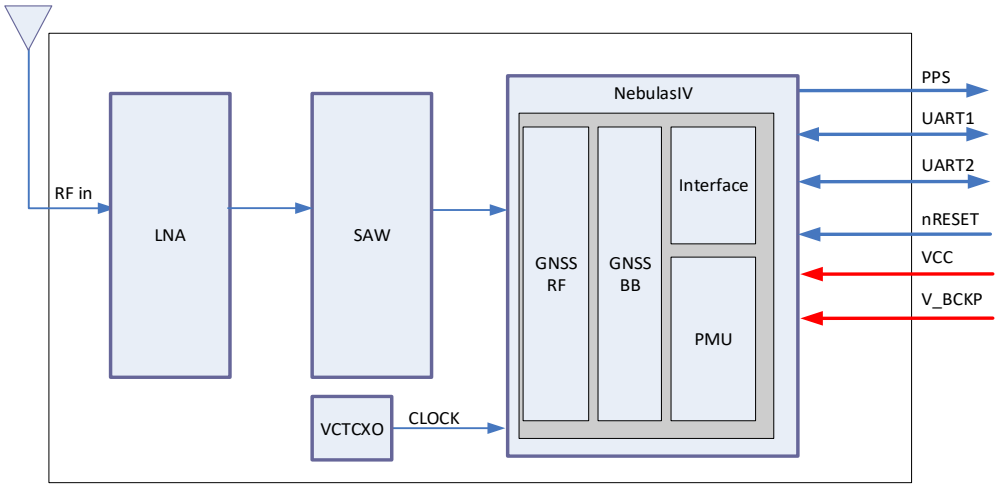


Figure 1-2 UT986 Block Diagram

- RF Part

The receiver gets filtered and enhanced GNSS signal from the antenna via a coaxial cable. The RF part converts the RF input signals into the IF signals, and converts IF analog signals into digital signals required for NebulasIV™ chip.

- NebulasIV™ SoC

NebulasIV™ is UNICORECOMM's new generation high precision GNSS SoC with 22 nm low power design, supporting all constellations, multiple frequencies and 1408 super channels. It integrates a dual-core CPU, a high speed floating point processor and an RTK co-processor, which can fulfill the high precision baseband processing and RTK positioning independently.

- External Interfaces

The external interfaces of UT986 include UART, PPS, nRESET, etc.

### 1.3.1 Pulse per Second (1PPS)

UT986 provides one 1PPS signal output with adjustable pulse width and polarity, which can be configured and queried through the **CFGTP** command. **TIMTP** is used to describe the related 1PPS information including the corresponding time and time accuracy indicators.

The 1PPS signal of UT986 is the output for timing, which is an important functional signal, and needs to be connected to the time scale input interface of the host. The output period of 1PPS is 1 s, and the default duty cycle is 10%.

## 1.3.2 Serial Port

The two serial ports of UT986 are LVTTL, which need to be converted through RS232 level if connected to a PC.

The UART1 is the master port. It supports the data transmission and firmware upgrade. The default baud rate is 460800 bps, and it can be configured by users. When designing products, make sure that UART1 is connected to a PC or external processor to support firmware upgrade.

The UART2 is an optional port, only for backup. It only supports data transmission and is unavailable for firmware upgrade. The port can be connected or unconnected depending on the situation.

It is recommended to reserve a test point for UART2 as the debug port.

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☞If there is data input at the digital IO (including RXD1, TXD1, RXD2, TXD2, TIME PULSE, and nRESET) when the module is not powered on, it will form a leakage on the VCC. And if the leakage voltage is higher than 0.4 V, it may cause a start failure when the module is powered on. Therefore, in order to prevent the leakage, ensure that the IO ports connected to the module are in high impedance or low level before the module is powered on.

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### 1.3.3 Clock

The industrial VCTCXO is built in UT986 to ensure the stability of the clock system and the ability to capture signals quickly in weak signal environments.

### 1.3.4 nRESET Timing Requirement

The module's reset pin nRESET and power supply VCC should meet the following requirement of time sequence when powering up. During its normal operation, pulling down the nRESET pin for more than 2.5 ms can also reset the UT986 module.

The reset pin nRESET is effective when lower than 0.3 V.

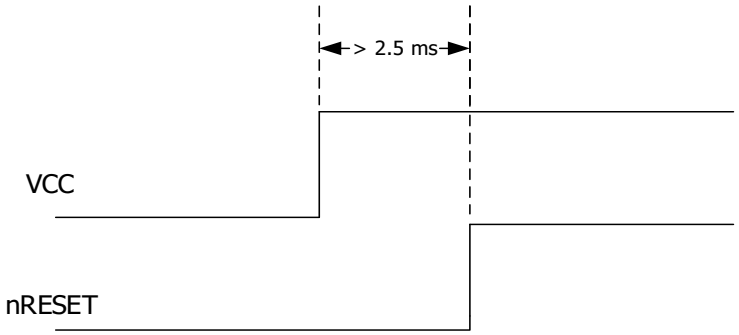



Figure 1-3 UT986 Reset Signal

### 1.3.5 Antenna

The filter and linear amplifier are built in the UT986 module. It is recommended to use an active antenna to provide better performance.

The antenna should support signal frequencies ranging from 1160 MHz to 1230 MHz and 1555 MHz to 1610 MHz, support right-handed circular polarization, and the output VSWR should be ≤ 2.0, gain range should be within 5 dB to 35 dB, in-band flatness < 1.5, out-of-band suppression >50 dB @2G3G4G5G communication frequencies.

## 1.4 Precision Timing and Raw Data Output

UT986 supports fixed-location timing, optimized-location timing, and positioning timing. Switch or query the above timing modes through **CFGTM** command. The module can simultaneously track all the four GNSS systems including GPS, BDS, GLONASS and Galileo, and can be switched back and forth between these four systems using **CFGGNSS** command.

The default mode of UT986 module is optimized-location timing. It outputs information of the dynamic position and fixed position, which can be queried by **TIMPOS** command. Refer to *Unicore Timing Products Protocol Specification* for more details.

**Fixed-location Timing**

Fixed-location timing mode only applies to static scenes. In this mode, users are required to input the exact position of the receiver's antenna center through the **CFGTM** command. UT986 uses this position to calculate the distance between the antenna and satellites, and calculate time to provide timing service.

**Optimized-location Timing**

Optimized-location timing mode also applies to static scenes. In this mode, the receiver collects a number of positioning points (within observation time) and calculates the exact position of the antenna. After that, the position is locked down, the timing mode is switched to fixed-location timing, and the receiver provides timing based on the locked position.

The observation time and accuracy are configured through **CFGTM** command. The fixed-location timing mode is activated only after both of them are configured. Query the observation status through **TPFINFO** command.

Using the **CFGTM** command, the calculated position of the antenna can be saved or not. For the former, the position estimation process only needs to be done once after UT986 is installed; and for the latter, the process does again after the restart. After the optimization of the position, the timing mode of the receiver automatically switches to the fixed-location timing mode.

☞ If the position of UT986 antenna changes, the command **CFGTM** must be sent again to switch the timing mode back to the optimized-location timing mode to recalibrate the antenna position. Refer to *GNSS Timing Products Protocol Specification* for more details.

**Positioning Timing**

In the positioning timing mode, UT986 calculates the antenna position and time in real time. It is the only mode that supports dynamic timing, and the timing quality depends on the satellite environment, which makes it difficult to guarantee the timing accuracy.

## 1.5 Protocols

Table 1-3 Supported Interface Protocols

| Protocol | Type |
|---|---|
| NMEA0183 | I/O, ASCII, NMEA4.1, NMEA4.11(Default output) |
| Unicore Protocol | I/O, ASCII, Unicore Protocol |
| RTCM[6] | Input, RTCM3.2 |

[6] For more information, please refer to *GNSS Timing Products Protocol Specification*

# 2 Installation for Test

This section describes how to use the EVK to test and evaluate the performance of the UT986 module.

To ensure a successful installation, please prepare the following accessories in advance:

- UT986 EVK (including a power supply)
- Matching antenna
- Antenna cable
- Straight-through cable
- Desktop or laptop computer with serial port and UPrecise.

☞Please keep the packing box and antistatic box for storage and handling.

## 2.1 Attentions

Many components on the UT986 module are static sensitive devices (SSD). Therefore, it is necessary to provide ESD protection for IC circuits and other SSD. Please obey all the ESD precautions and procedures.

- Electrostatic discharge (ESD) may cause damage to the device. All operations mentioned in this chapter should be carried out on an antistatic workbench using an antistatic wrist strap and conductive foam pad. If there is no antistatic workbench, wear an antistatic wrist strap and connect the other end of the strap to the metal frame to avoid electrostatic damages.
- Hold the edge of the evaluation board, and do NOT touch the components directly.

Carefully check the board to make sure that there is no apparent loose or damaged components. If you have any questions, please contact Unicore or the local distributors.

Figure 2-1 shows the typical installation of UT986 EVK.

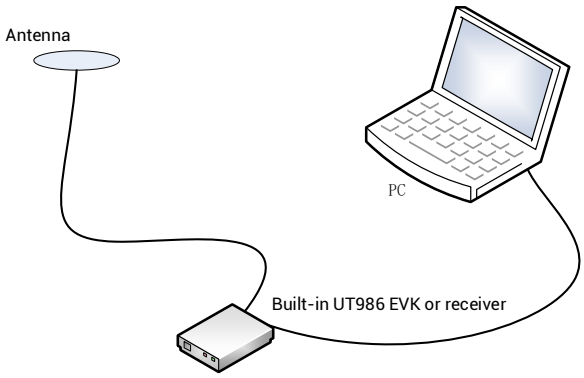



Figure 2-1 Typical Installation of UT986

## 2.2 Installation

After the above preparation, please follow the steps below to install.

Step1. Ensure adequate antistatic measures, such as wearing a grounded antistatic wrist strap, using a grounded workbench, etc.

Step2. Open UT986 EVK and take out the evaluation board.

Step3. Select the GNSS antenna with appropriate gain (the system frequency supported by the antenna should be consistent with the module), fix it in a non-occluded area, and use the appropriate cable to connect the antenna with the UT986 evaluation board.

Step4. Connect PC to COM1 or COM2 of the evaluation board with a straight-through cable.

Step5. Power on the evaluation board and initialize UT986.

Step6. Open the UPrecise software.

Step7. Control the receiver via UPrecise to display constellations view, messages, the receiver's status, etc.

# 3 Hardware

## 3.1 Pin Definition

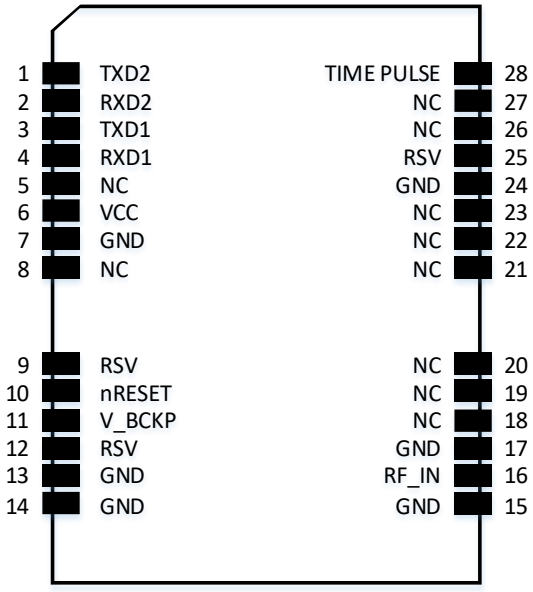



Figure 3-1 UT986 Pin Assignment

Table 3-1 Pin Definition

| No. | Name | I/O | Electrical Level | Description |
|---|---|---|---|---|
| 1 | TXD2 | O | LVTTL | COM2 for data transmission. Firmware upgrade is not supported. Leave this pin floating if idle. |
| 2 | RXD2 | I | LVTTL | COM2 for data reception. Firmware upgrade is not supported. Leave this pin floating if idle. |
| 3 | TXD1 | O | LVTTL | COM1 for data transmission. Firmware upgrade is supported. |
| 4 | RXD1 | I | LVTTL | COM1 for data reception. Firmware upgrade is supported. |
| 5 | NC | | | No connection inside |
| 6 | VCC | I | 3.0 V to 3.6 V | Power supply |
| 7 | GND | — | | Ground |
| 8 | NC | | | No connection inside |
| 9 | RSV | | | Reserved (recommended to be floating) |
| 10 | nRESET | I | LVTTL | External reset pin, active low |

| No. | Name | I/O | Electrical Level | Description |
|---|---|---|---|---|
| 11 | V_BCKP[7] | I | 2.0 V to 3.6 V | When the main power supply VCC is cut off, V_BCKP supplies power to RTC and relevant register. Level requirement: 2.0 V ~ 3.6 V, and the working current is less than 60 μA at 25 °C. If you do not use the hot start function, connect V_BCKP to VCC. Do NOT connect it to ground or leave it floating. |
| 12 | RSV | | | Reserved (recommended to be floating) |
| 13 | GND | — | | Ground |
| 14 | GND | — | | Ground |
| 15 | GND | — | | Ground |
| 16 | RF_IN | I | | GNSS signal input |
| 17 | GND | — | | Ground |
| 18 | NC | | | No connection inside |
| 19 | NC | | | No connection inside |
| 20 | NC | | | No connection inside |
| 21 | NC | | | No connection inside |
| 22 | NC | | | No connection inside |
| 23 | NC | | | No connection inside |
| 24 | GND | — | | Ground |
| 25 | RSV | | | Reserved (must be floating) |
| 26 | NC | | | No connection inside |
| 27 | NC | | | No connection inside |
| 28 | TIME PULSE | O | LVTTL | 1PPS (Leave this pin floating if idle.) |

[7] Not supported currently; future versions will support.

## 3.2 Electrical Specifications

### 3.2.1 Absolute Maximum Ratings

Table 3-2 Absolute Maximum Ratings

| Parameter | Symbol | Min. | Max. | Unit | Condition |
|---|---|---|---|---|---|
| Power Supply Voltage | VCC | -0.5 | 3.6 | V | |
| Backup Power Supply Voltage | V_BCKP | -0.5 | 3.6 | V | |
| Input Pin Voltage | $V_{in}$ | -0.5 | VCC + 0.2 | V | |
| Storage Temperature | $T_{stg}$ | -40 | 95 | °C | |
| Maximum ESD Stress | VESD (HBM) | | 2000 | V | All pins |

### 3.2.2 Operational Conditions

Table 3-3 Operational Conditions

| Parameter | Symbol | Min. | Typical | Max. | Unit | Condition |
|---|---|---|---|---|---|---|
| Power Supply Voltage | VCC | 3.0 | 3.3 | 3.6 | V | |
| VCC Maximum Ripple | $V_{rpp}$ | 0 | | 50 | mV | |
| Peak Current | $I_{ccp}$ | | | 600 | mA | VCC = 3.3 V |
| Backup Power Supply Voltage | V_BCKP | 2.0 | | 3.6 | V | |
| Operating Temperature | $T_{opr}$ | -40 | | 85 | °C | |

### 3.2.3 IO Threshold Values

Table 3-4 IO Threshold Values

| Parameter | Symbol | Min. | Typical | Max. | Unit | Condition |
|---|---|---|---|---|---|---|
| Low Level Input Voltage | $V_{in\_low}$ | 0 | | VCC × 0.2 | V | |
| High Level Input Voltage | $V_{in\_high}$ | VCC × 0.7 | | VCC + 0.2 | V | |
| Low Level Output Voltage | $V_{out\_low}$ | 0 | | 0.45 | V | $I_{out}$ = 4 mA |
| High Level Output Voltage | $V_{out\_high}$ | VCC - 0.45 | | VCC | V | $I_{out}$ = 4 mA |
| nRESET Low Level Voltage | $V_{nrst\_low}$ | 0 | | 0.3 | V | |

### 3.2.4 Antenna Characteristics

Table 3-5 Antenna Characteristics

| Parameter | Symbol | Min. | Typical | Max. | Unit | Condition |
|---|---|---|---|---|---|---|
| Antenna Gain | $G_{ant}$ | 5 | | 35 | dB | |

## 3.3 Dimensions

Table 3-6 Dimensions

| Parameter | Min. (mm) | Typical (mm) | Max. (mm) |
|---|---|---|---|
| A | 22.20 | 22.40 | 22.90 |
| B | 16.80 | 17.00 | 17.50 |
| C | 2.2 | 2.4 | 2.6 |
| D | 2.75 | 2.85 | 2.95 |
| E | 1.00 | 1.10 | 1.20 |
| F | 3.70 | 3.80 | 3.90 |
| G | 2.45 | 2.55 | 2.65 |
| H | 0.72 | 0.82 | 0.92 |
| J | 1.90 | 2.00 | 2.10 |
| K (Outer edge of the stamp hole) | 0.70 | 0.80 | 0.90 |
| M | 0.90 | 1.00 | 1.10 |
| N (Inner edge of the stamp hole) | Φ0.40 | Φ0.50 | Φ0.60 |
| P | 5.10 | 5.20 | 5.30 |
| R | 4.40 | 4.50 | 4.60 |
| X | 0.90 | 1.00 | 1.10 |

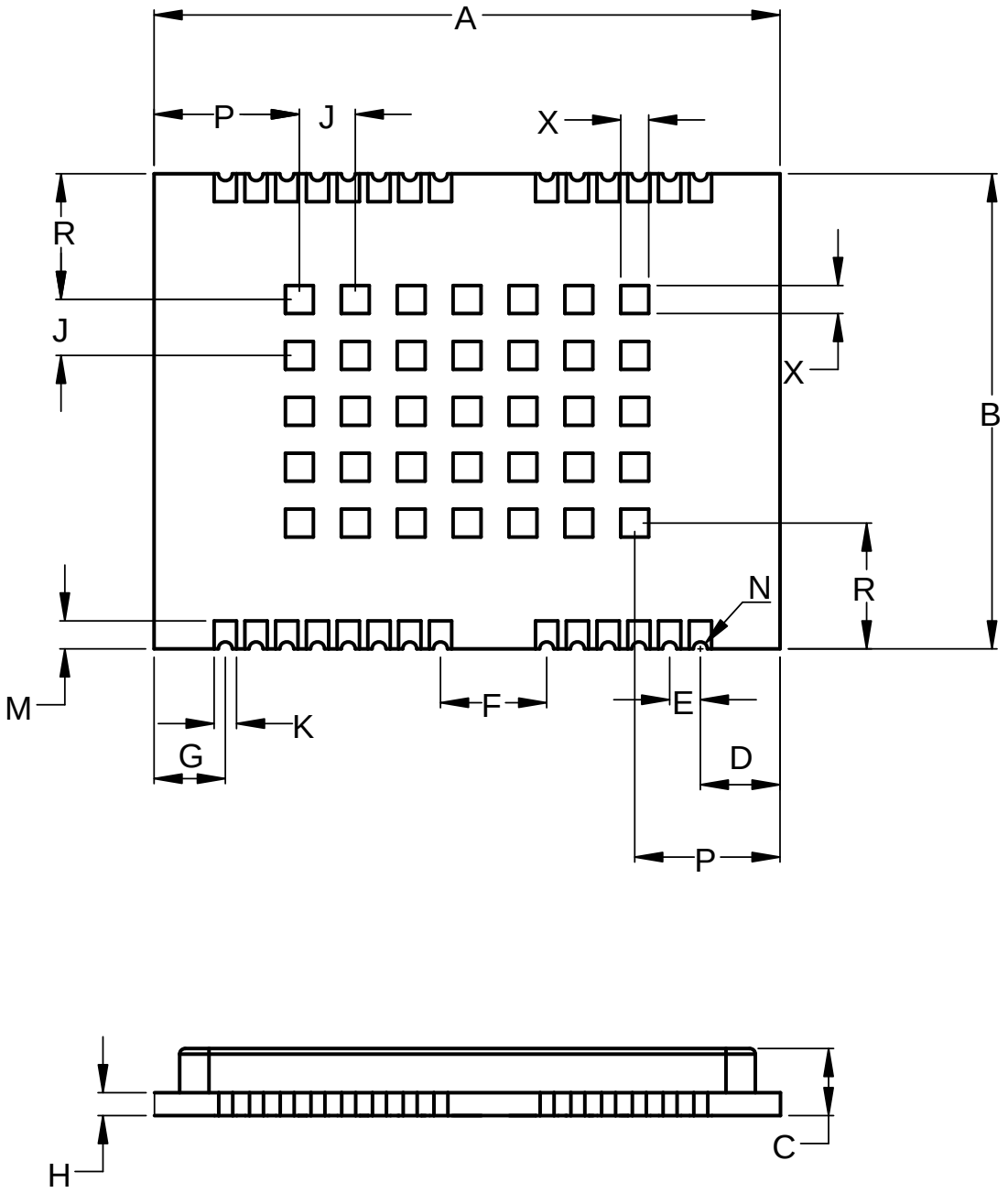



Figure 3-2 Mechanical Layout

# 4 Hardware Design

## 4.1 Recommended Minimal Design

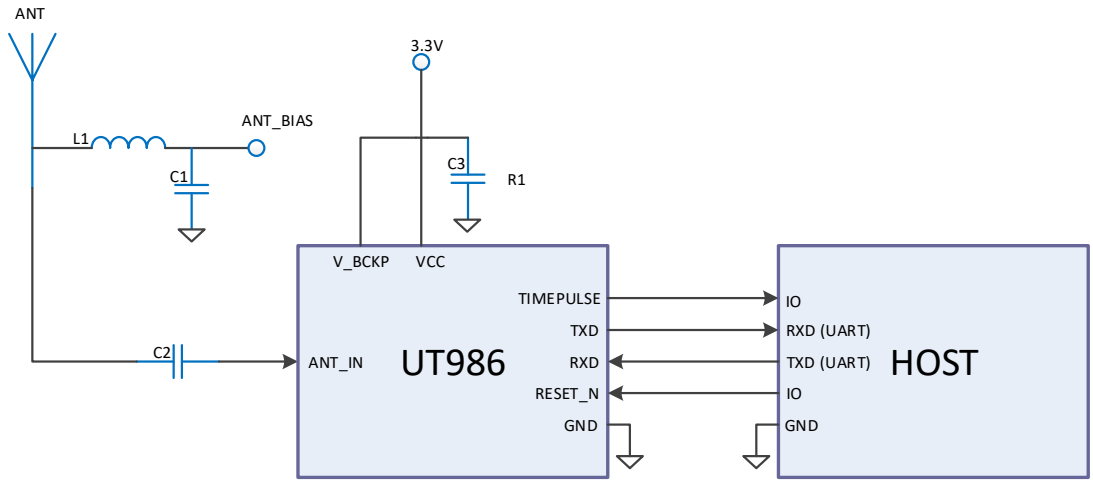



Figure4-1 UT986 Minimal Design

**Remarks:**

- L1: 68 nH RF inductor in 0603 package is recommended
- C1: 100 nF + 100 pF capacitors connected in parallel is recommended
- C2: 100 pF capacitor is recommended
- C3: n × 10 μF + 1 × 100 nF capacitors connected in parallel is recommended, and the total inductance should be no less than 30 μF
- R1: 10 kΩ resistor is recommended

## 4.2 Antenna Feed Design

UT986 just supports feeding the antenna from the outside of the module rather than from the inside. It is recommended to use devices with high power and that can withstand high voltage. Gas discharge tube, varistor, TVS tube and other high-power protective devices may also be used in the power supply circuit to further protect the module from lightning strike and surge.

⚠ If the antenna feed supply ANT_BIAS and the module's main supply VCC use the same power rail, the ESD, surge and overvoltage from the antenna will have an effect on VCC, which may cause damage to the module. Therefore, it is recommended to design an independent power rail for the ANT_BIAS to reduce the possibility of module damage.

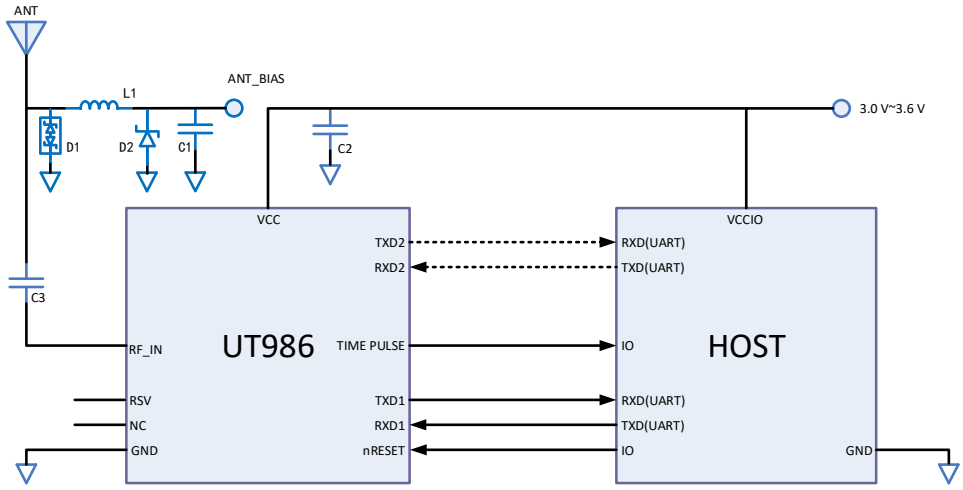



Figure 4-2 UT986 Reference Circuit

**Remarks:**

- L1: feed inductor, 68 nH RF inductor in 0603 package is recommended. The rated current of the L1 inductor should be larger than the operating current of the selected antenna, and leave enough design margin
- C1: decoupling capacitor, recommended to connect two capacitors of 100 nF/100 pF in parallel
- C3: DC blocking capacitor, recommended 100 pF capacitor
- D1: ESD diode, choose the ESD protection device that supports high frequency signals (above 1000 MHz)
- D2: TVS diode, choose the TVS diode with appropriate clamping specification according to the requirement of feed voltage and antenna voltage
- RF_IN does not feed the antenna. You need to design the antenna feed circuit according to the antenna you choose.

## 4.3 Power On and Power Off

**VCC**

- The VCC initial level when power-on should be less than 0.4 V.
- The VCC ramp when power-on should be monotonic, without plateaus.
- The voltages of undershoot and ringing should be within 5% VCC.
- VCC power-on waveform: The time interval from 10% rising to 90% must be within 100 μs to 1 ms.
- Power-on time interval: The time interval between the power-off (VCC < 0.4 V) to the next power-on must be larger than 500 ms.
- It is recommended to use the same power supply for the VCC of UT986 and the IO of the host, so as to avoid abnormal startup caused by the IO leakage between UT986 and the host. The power supply of UT986 VCC ranges from 3.0 V to 3.6 V, and the input decoupling capacitor C2 (see Figure 4-2) needs to be more than 10 μF. Other capacitors, such as 1 μF/100 nF/ 100 pF, can be connected in parallel.

**V_BCKP**

- The V_BCKP initial level when power-on should be less than 0.4 V.
- The V_BCKP ramp when power-on should be monotonic, without plateaus.
- The voltages of undershoot and ringing should be within 5% V_BCKP.
- V_BCKP power-on waveform: The time interval from 10% rising to 90% must be within 100 μs to 1 ms.
- Power-on time interval: The time interval between the power-off (V_BCKP < 0.4 V) to the next power-on must be larger than 500 ms.

## 4.4 Grounding and Heat Dissipation

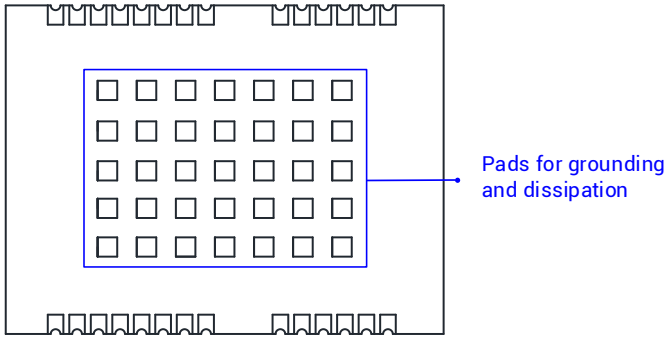



Figure 4-3 Pads for grounding and dissipation

There are 35 pads in the middle rectangle area of UT986 module, which are used for grounding and heat dissipation. When designing PCB, connect the pads to a large size of ground to facilitate heat dissipation.

## 4.5 Recommended PCB Package Design

See the following figure for the recommended PCB package design of the module UT986.

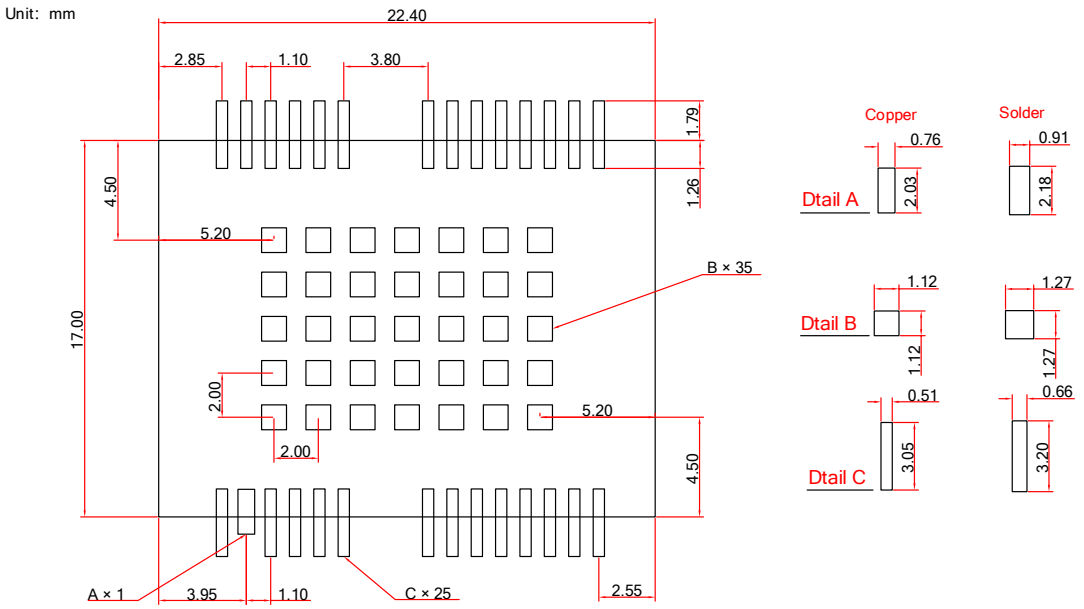



Figure 4-4 Recommended PCB Package Design

**Remark:**

- For the convenience of testing, the soldering pads of the pins are designed long, exceeding the module border much more. For example:
  - ✓ The pads denoted as detail C are 1.79 mm longer than the module border.
  - ✓ The pad denoted as detail A is 0.77 mm longer than the module border. It is relatively short as it is an RF pin pad, so we hope the trace on the surface is as short as possible to reduce the impact of interference.
- In order to effectively reduce the possibility of solder bridge during the soldering, the pin pads are designed narrower than the pins. However, the pad denoted as detail A has the same width as the pin, as we hope the resistance is as continuous as possible at the RF pin.

## 4.6 Layout Recommendation

- Power supply: Stable and low ripple power is necessary for good performance. Make sure the peak-to-peak ripple voltage does not exceed 50 mV.
  - Use LDO to ensure the purity of power supply
  - Place LDO as close to the module as possible in layout
  - Widen the power circuit wiring or use split copper surface to transmit current
  - Keep away from any high power or high inductance devices such as a magnetic coil.
- Antenna link: The antenna link requires 50 Ω impedance matching. The RF routing connecting RF_IN and the antenna should have 50 Ω impedance, as short and smooth as possible, and avoid acute angles.
- Antenna location: In order to obtain a good signal-to-noise ratio, ensure that the antenna is well isolated from electromagnetic radiation sources, especially electromagnetic radiation in the frequency range of 1100 MHz to 1610 MHz.
- Try to avoid circuits below UT986 module.
- UT986 is a temperature sensitive device and rapid temperature changes can result in reduced performance. Keep it away as far as possible from any high-temperature air and high-power heating devices.
- Connect all the GND pins of UT986 to the ground.
- All the RSV pins are reserved and it is recommended to keep them floating.
- The thermal pad of UT986 must be connected to a large area of grounding copper to effectively dissipate heat.

# 5 Production Requirement

## 5.1 Disassembly

When disassembling the module, it is recommended to melt the soldering tin of the pins on both sides of the module with an electric soldering iron and remove the module with a tweezer. Do NOT use other means to remove the module (for example, blow off the module with a hot air gun), which may damage the module.

## 5.2 Clean

Do NOT use alcohol or other organic solvents to clean the module, or it may lead to flux residues entering into the shielding shell, causing mildew and other problems.

## 5.3 Reflow Soldering

- In order to prevent falling off during soldering of the module, do not solder it on the back of the board during design, and it is not recommended to go through soldering cycle twice.
- The setting of soldering temperature depends on many factors of the factory, such as board type, solder paste type, solder paste thickness, etc. Please also refer to the relevant IPC standards and indicators of solder paste.
- Since the lead soldering temperature is relatively low, if using this method, please give priority to other components on the board.
- The opening of the stencil needs to meet your design requirement and comply to the examine standards. The thickness of the stencil must be larger than 0.15 mm and it is recommended to be larger than 0.18 mm.

The recommended reflow temperature curve is shown in the figure below.

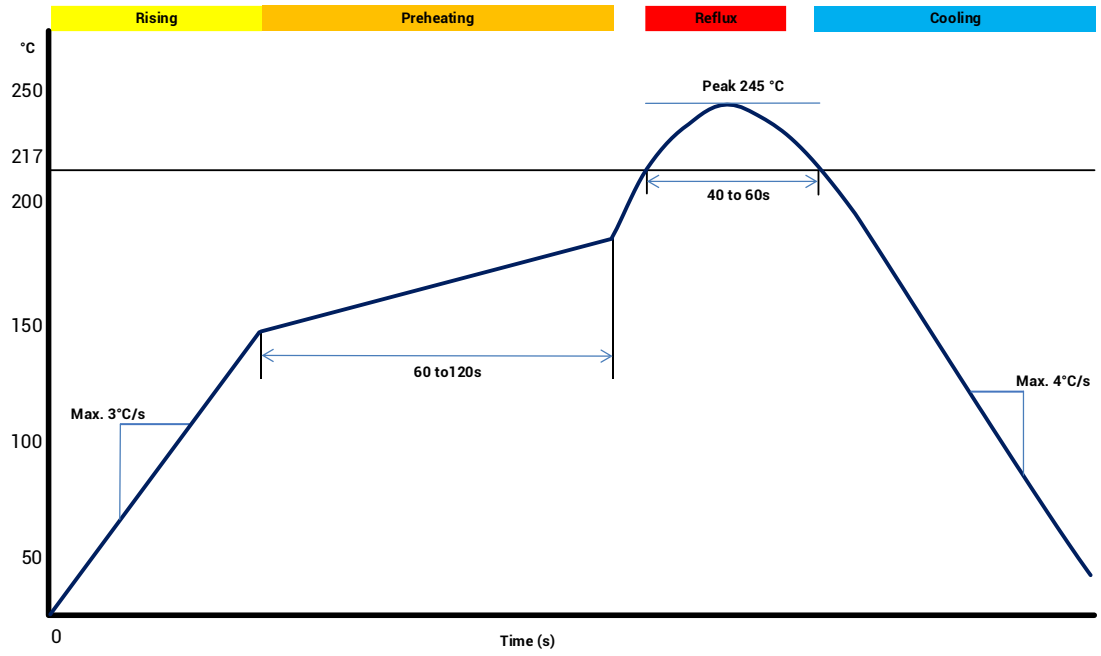



Figure 5-1 (M705-GRN360) Reflow Soldering Temperature Curve

**Temperature Rising Stage**

- Rising slope: Max. 3 °C/s
- Rising temperature range: 50 °C to 150°C

**Preheating Stage**

- Preheating time: 60 s to 120 s
- Preheating temperature range: 150 °C to 180 °C

**Reflux Stage**

- Over melting temperature (217 °C) time: 40 s to 60 s
- Peak temperature for soldering: No higher than 245 °C

**Cooling Stage**

- Cooling slope: Max 4 °C/s

# 6 Packaging

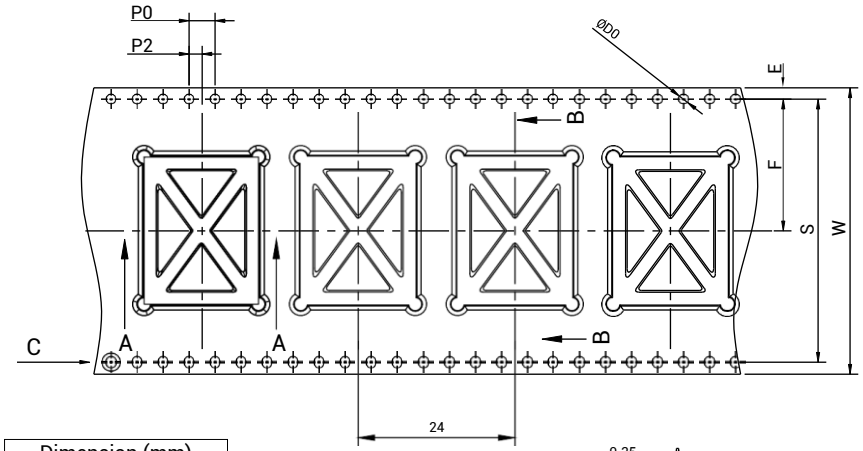
## 6.1 Product Label


Figure 6-1 Product Label

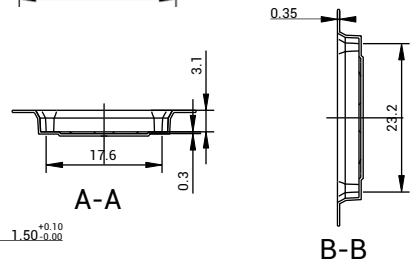
## 6.2 Packaging Description

UT986 module uses carrier tape and reel (suitable for mainstream surface mount devices), packaged in vacuum-sealed aluminum foil antistatic bags, with a desiccant inside to prevent moisture. When using reflow welding process to weld modules, please strictly comply with IPC standard to conduct humidity control on the modules. As packaging materials such as carrier tape can only withstand the temperature of 55 °C, modules should be removed from the package during baking.

Figure 6-2 Packaging Diagram

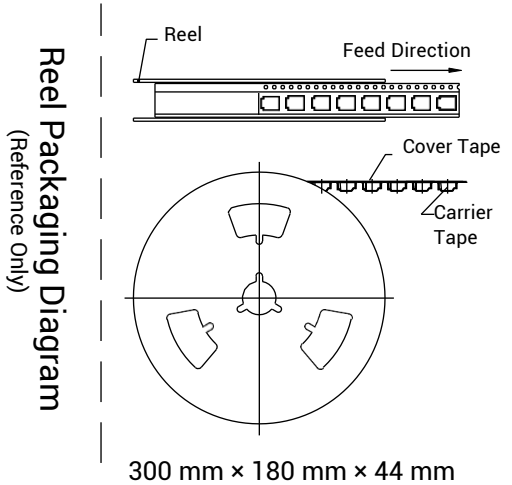



| Dimension (mm) | |
|---|---|
| E | 1.75 ±0.10 |
| F | 20.20 ±0.10 |
| S | 40.40 ±0.10 |
| P2 | 2.00 ±0.10 |
| ΦDo | $1.50 \pm {}^{0.10}_{0.00}$ |
| ΦD1 | |
| Po | 4.00 ±0.10 |
| 10Po | 40.00 ±0.20 |
| W | 44.00 ±0.30 |
| P | 24.00 ±0.10 |
| Ao | 17.60 ±0.10 |
| B0 | 23.20 ±0.10 |
| K0 | 3.10 ±0.10 |
| t | 0.35 ±0.05 |

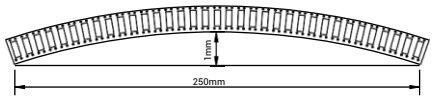



**Note:**

- The cumulative tolerance of 10 side holes should not exceed ±0.2 mm.
- Material: Black antistatic PS (surface impedance $10^5$-$10^{11}$) (surface static voltage <100 V), thickness: 0.35 mm.
- Total length of the 13-inch reel package: 6.816 m (Length of the first part of empty packets: 0.408 m, length of packets containing modules: 6 m, length of the last part of empty packets: 0.408 m).
- Total number of packets in the 13-inch reel package: 284 (Number of the first part of empty packets: 17; actual number of modules in the packets: 250; number of the last part of empty packets: 17).




- All dimension designs are in accordance with EIA-481-C-2003.
- The maximum bending degree of the carrier tape within the length of 250 mm should not exceed 1mm (see the figure below).




(Unit: mm)

Figure 6-3 Carrier Tape Drawing

Table 6-1 Packaging Description

| Item | Description |
|---|---|
| Modules | 250 pieces/reel |
| Reel Size | Tray: 13"<br>External diameter: 330 ±2 mm,<br>Internal diameter: 180 ±2mm,<br>Width of internal diameter: 44.5 ±0.5 mm,<br>Thickness: 2.0 ±0.2 mm |
| Carrier Tape | Module spacing (center to center distance): 24 mm |

UT986 module is rated at MSL level 3. For more information about packaging and handling precautions related to the Moisture Sensitivity Level, please refer to the IPC/JEDEC J-STD-033 standards. Users may access to the website www.jedec.org to find out more details.

The shelf life of the UT986 module packaged in vacuum-sealed aluminum foil antistatic bags is one year.

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